BUK725R0-40C

N-channel TrenchMOS standard level FET

Rev. 01 — 23 March 2009 | Product data sheet

1. Product profile

1.1 General description

Standard level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Avalanche robust
- Suitable for standard level gate drive
- Suitable for thermally demanding environment up to 175°C rating

1.3 Applications

- 12V Motor, lamp and solenoid loads
- High performance automotive power systems
- High performance Pulse Width Modulation (PWM) applications

1.4 Quick reference data

Table 1. Quick reference

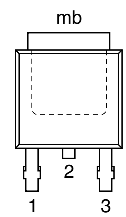
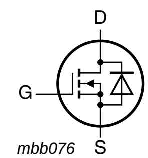
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 3;	[1]	-	-	75	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	-	157	W
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped		-	-	240	mJ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 25$ A; $V_{DS} = 32$ V; $T_j = 25$ °C; see Figure 15		-	27	-	nC
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 12; see Figure 13		-	4.1	5	mΩ

[1] Current is limited by package.

founded by Philips

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 **SOT428 (SC-63; DPAK)**	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK725R0-40C	SC-63; DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3;	[1]	-	75	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; see Figure 1	[1]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 3		-	490	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	157	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25$ °C;	[2]	-	75	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C		-	490	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped		-	240	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 4	[3][4][5]	-	-	J

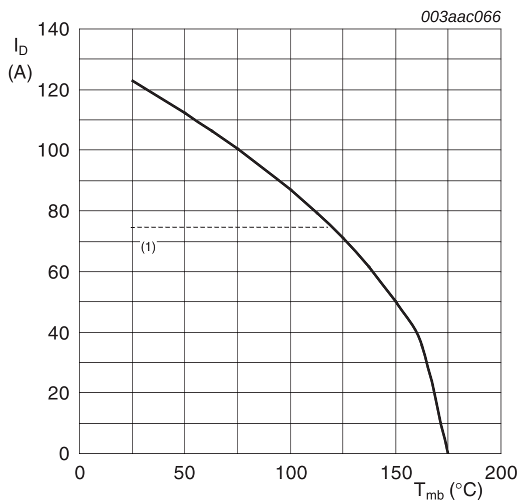
[1] Current is limited by package.

[2] Continuous current is limited by package.

[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[4] Repetitive avalanche rating limited by average junction temperature of 170 °C.

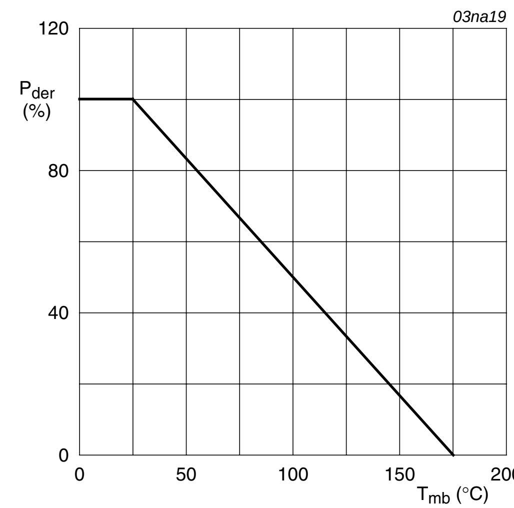
[5] Refer to application note AN10273 for further information.



$V_{GS} \geq 10\,V$

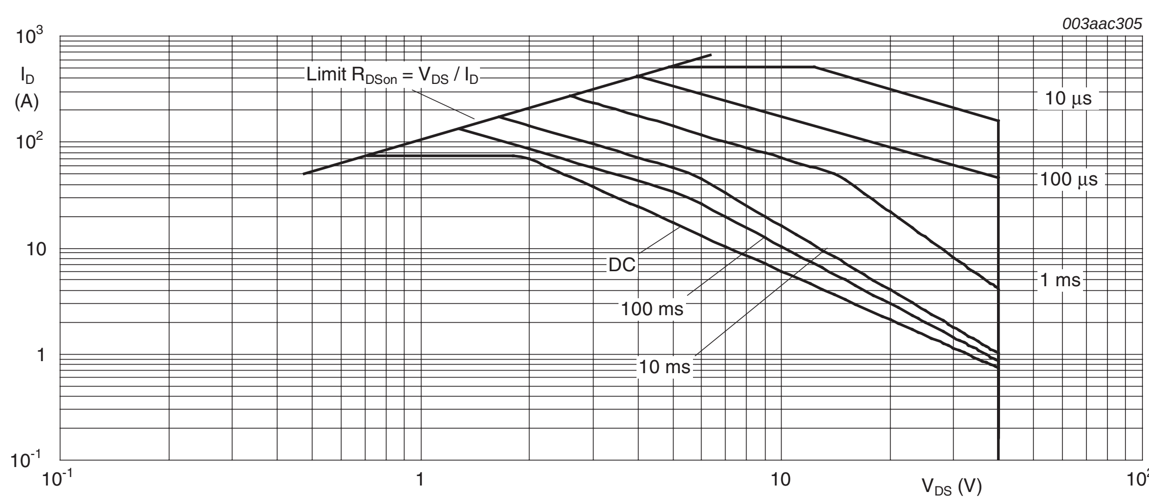
(1) Capped at 75 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

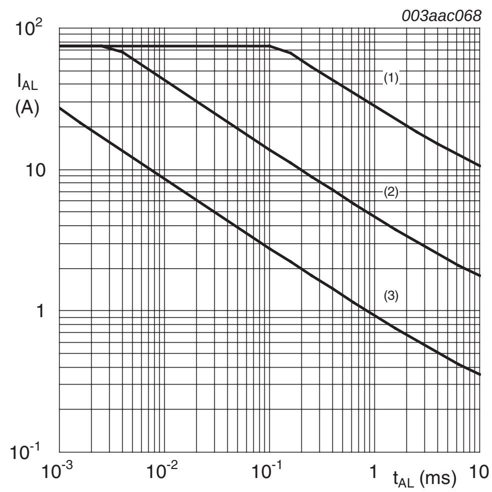
Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25\,°C$; I_{DM} is single pulse

Capped at 75 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) Single-pulse; $T_j = 25\,°C$.
(2) Single-pulse; $T_j = 150\,°C$.
(3) Repetitive.

Fig 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	0.65	0.95	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; mounted on a printed circuit board; minimum foot-print	-	70	-	K/W

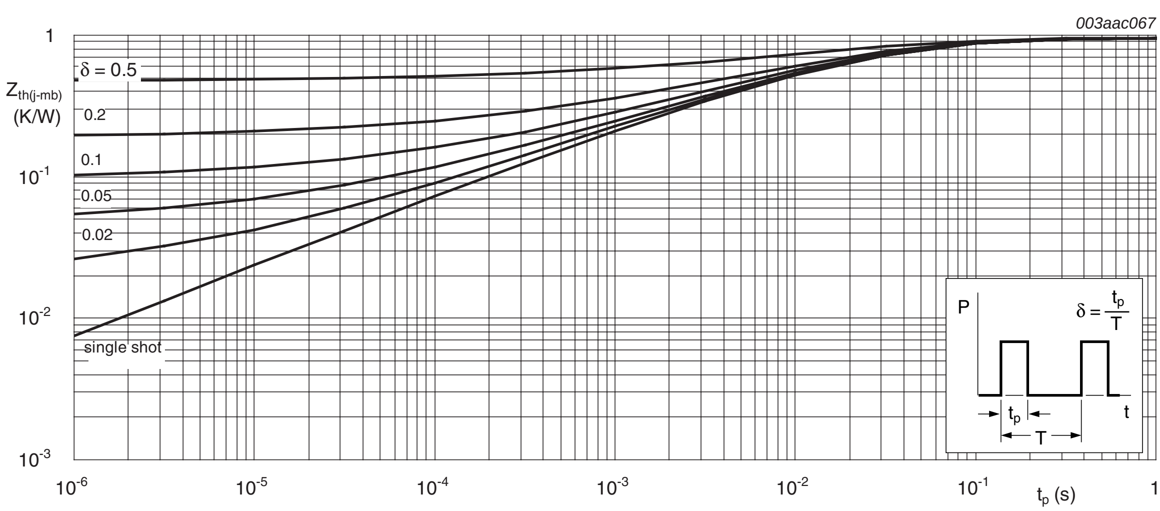
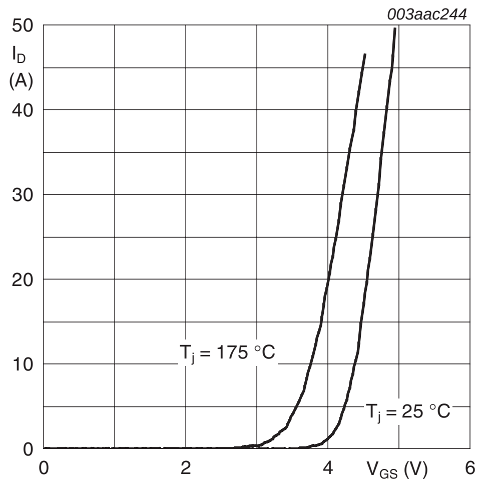


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

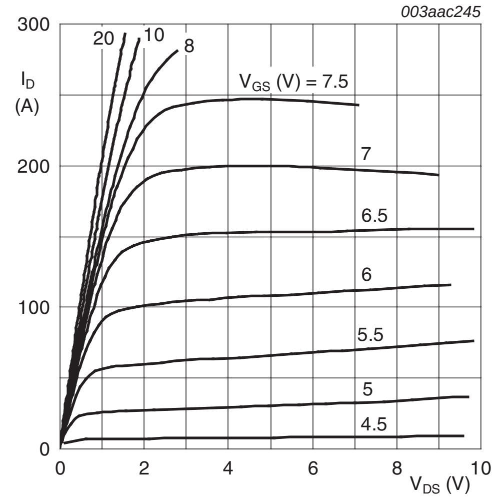
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10	-	-	4.4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	2	3	4	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	1	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 12	-	-	9.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 12; see Figure 13	-	4.1	5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 15	-	60	-	nC
Q_{GS}	gate-source charge		-	12	-	nC
Q_{GD}	gate-drain charge		-	27	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	2870	3820	pF
C_{oss}	output capacitance		-	540	650	pF
C_{rss}	reverse transfer capacitance		-	350	490	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	27	-	ns
t_r	rise time		-	73	-	ns
$t_{d(off)}$	turn-off delay time		-	82	-	ns
t_f	fall time		-	63	-	ns
L_D	internal drain inductance	measured from drain to centre of die; T_j = 25 °C	-	2.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad; T_j = 25 °C	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 14	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	50	-	ns
Q_r	recovered charge		-	25	-	nC



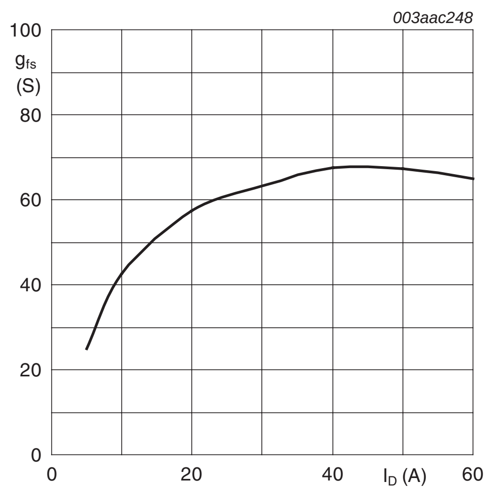
$V_{DS} = 25 V$

Fig 6. **Transfer characteristics: drain current as a function of gate-source voltage; typical values**



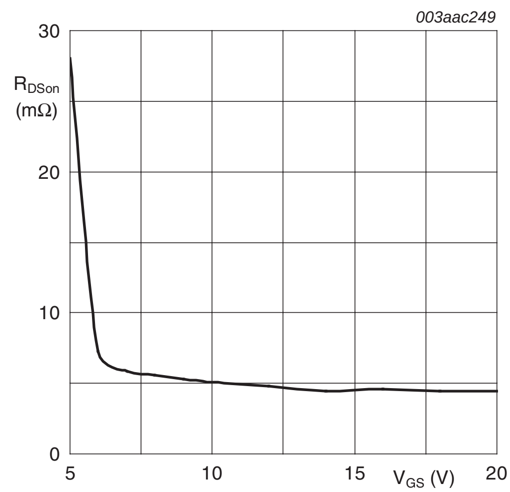
$T_j = 25 °C$

Fig 7. **Output characteristics: drain current as a function of drain-source voltage; typical values**



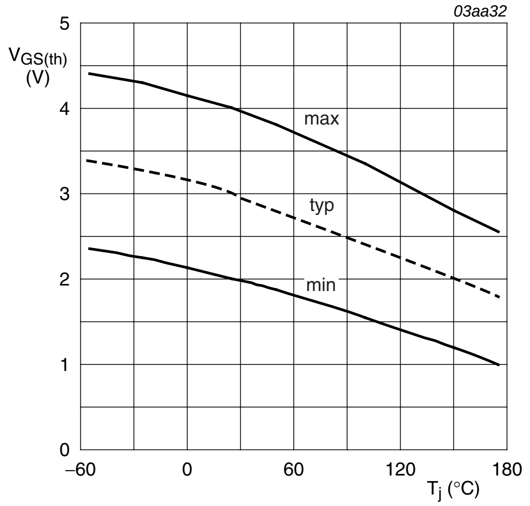
$T_j = 25 °C; V_{DS} = 25 V$

Fig 8. **Forward transconductance as a function of drain current; typical values**



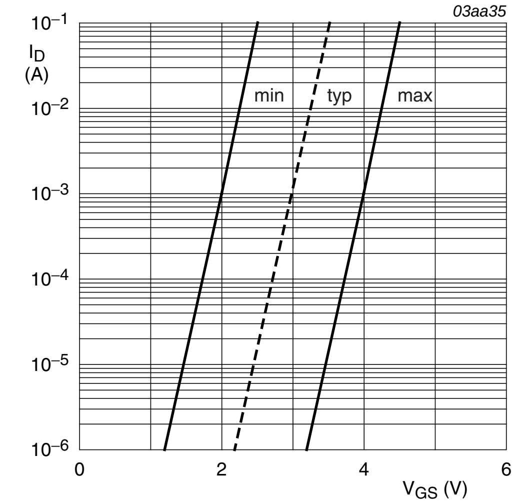
$T_j = 25 °C; I_D = 25 A$

Fig 9. **Drain-source on-state resistance as a function of gate-source voltage; typical values**



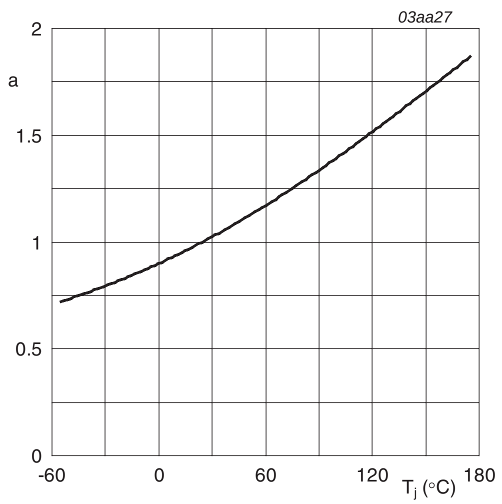
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



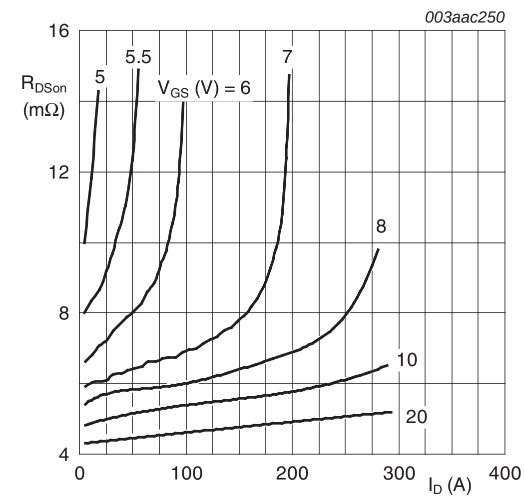
$T_j = 25\,°C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



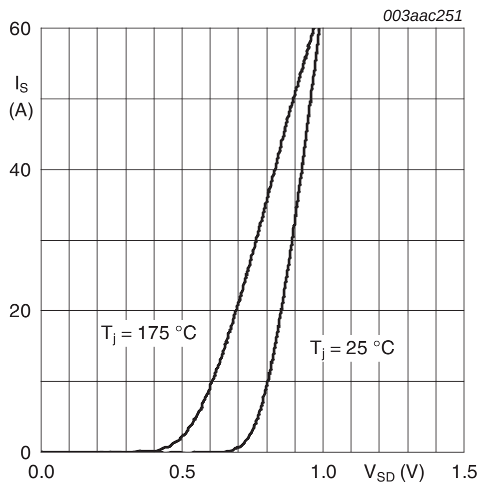
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



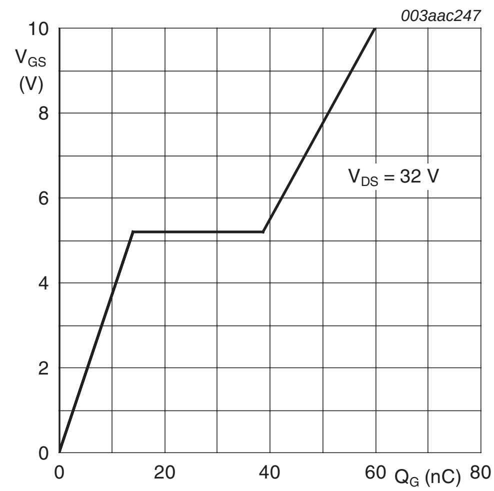
$T_j = 25\,°C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values



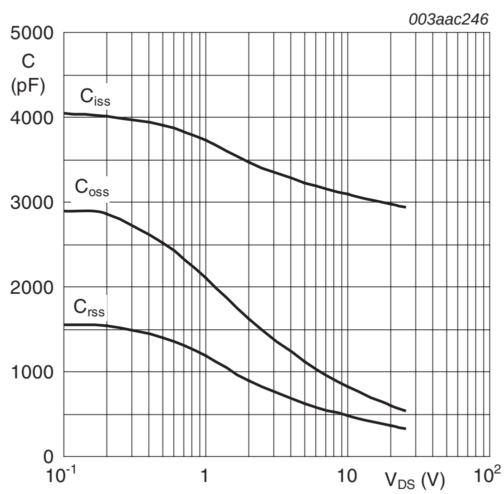
$V_{GS} = 0 V$

Fig 14. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



$T_j = 25 °C; I_D = 25 A$

Fig 15. Gate-source voltage as a function of gate charge; typical values

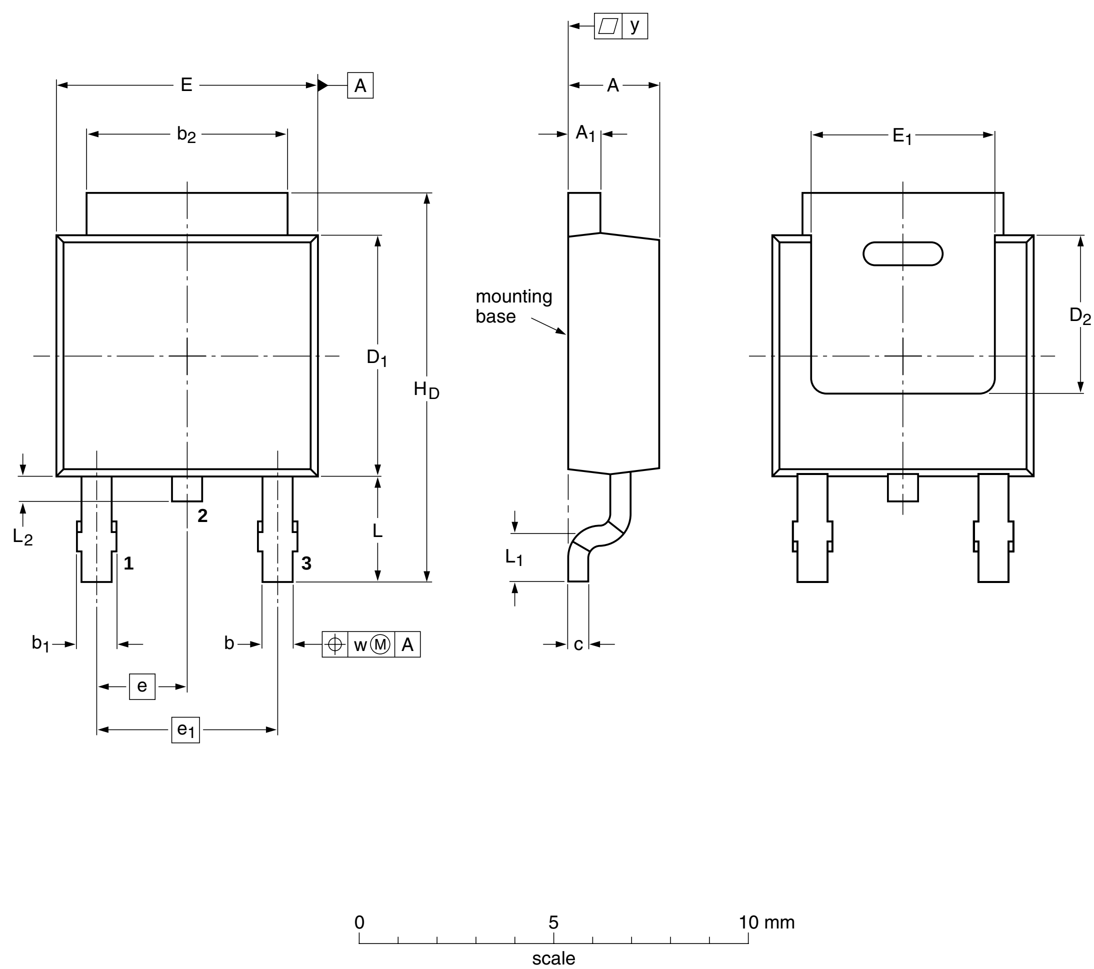


$V_{GS} = 0 V; f = 1 MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 17. Package outline SOT428 (DPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK725R0-40C_1	20090323	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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